What Is Claimed Is:

1. An apparatus for protecting a MOS component from the antenna effect, the apparatus comprising:

a bypass PMOS transistor, having a gate, a source and a substrate, all coupled to a first voltage node; wherein when positive charges are accumulated on the gate of the MOS component due to antenna effect, the bypass PMOS transistor conveys the positive charges to the first voltage node to prevent the positive charges from entering and damaging the MOS component; and

a bypass NMOS transistor, having a gate, a source and a substrate, all coupled to a second voltage node; when negative charges are accumulated on the gate of the MOS component due to antenna effect, the bypass NMOS transistor conveys the negative charges to the second voltage node to prevent the negative charges from entering and damaging the MOS component.

2. A method for protecting a MOS component from antenna effect, comprising:

Disposal, between a first voltage node and the MOS component, of a bypass PMOS transistor the gate, the source and substrate of which are coupled to the first voltage node and the drain of which is coupled to the gate of the MOS component; and

Disposal, between a second voltage node and the MOS component, of a bypass NMOS transistor the gate, source and substrate of which are coupled to the second voltage node and the drain of which is coupled to the gate of the MOS component;

wherein when positive charges are accumulated on the gate of the MOS component due to antenna effect, the bypass PMOS

transistor conveys the positive charges to the first voltage node to prevent the positive charges from entering and damaging the MOS component; when negative charges are accumulated on the gate of the MOS component due to antenna effect, the bypass NMOS transistor conveys the negative charges to the second voltage node to prevent the negative charges from entering and damaging the MOS component.